In view of the foregoing amendments and the following remarks, reconsideration and allowance are requested. Claims 1-30 are pending in the application after amendment, with claims 1 and 19 being independent. Claims 1-8, 10, 11, 13, 15, 16, 18-21, and 24-28 have been amended. Claims 29 and 30 have been added.

REMARKS

Claims 1-18 stand rejected under 35 USC 112, second paragraph for the reasons set forth on page 2 of the office action.

Claims 1-6, 16-17, 19, and 24-28 stand rejected under 35 USC 103(a) as allegedly being unpatentable over U.S. Patent Number 6,259,085 to Holland ("Holland") in view of U.S. Patent Number 5,510,285 to Kim ("Kim"). Claims 7-13 and 18 stand rejected under 35 USC 103(a) as allegedly being unpatentable over Holland and Kim, and further in view of U.S. Patent Number 5,381,013 to Cox et al. ("Cox"). Claims 20-21 stand rejected under 35 USC 103(a) as being unpatentable over Holland and Kim, and further in view of Cox. Claims 14-15 stand rejected under 35 USC 103(a) as allegedly being unpatentable over Holland, Kim, and Cox, and further in view of U.S. Patent Number 5,262,633 to Kasai et al. ("Kasai"). Claims 22-23 stand rejected under 35 USC 103(a) as allegedly being unpatentable over Holland, Kim, Cox, and Kasai.

These rejections, and their underlying rationale at pages 2-6 of the office action, are traversed.

I. The 35 USC 112 rejections

Claims 1-18 are rejected as allegedly being indefinite. The office action states that it is unclear how to bias the substrate with respect to the doped regions.

Applicants have amended claim 1 to recite:

1. (Amended) A semiconductor position-sensitive radiation detection device, comprising:

a substrate formed of a semiconductor material doped to exhibit a first conductivity type and configured to have first and second surfaces opposing each other, the substrate having a bias layer proximate to the first surface and electrically coupled to the substrate, and an array of doped gate regions of a second conductivity type proximate to the second surface; and

a grid of conducting wires proximate to and in electrical contact with the bias layer and configured to define an array of pixels corresponding to the array of doped gate regions;

wherein the grid of conducting wires is configured to be electrically coupled to a voltage source and to distribute a bias voltage on the bias layer so as to bias the substrate with respect to the doped gate regions.

According to claim 1, the substrate may be biased with respect to the doped gate regions by providing a bias voltage to the bias layer. The bias voltage may be provided by a voltage source electrically coupled to the grid of conducting wires, which distribute the bias voltage on the bias layer.

Accordingly, Applicants believe that claim 1 as amended satisfies the requirements of 35 USC 112, second paragraph.

II. The rejections under 35 USC 103(a)

Claim 1

Claim 1 stands rejected under 35 USC 103(a) as allegedly being obvious over Holland in view of Kim. Applicants disagree.

First, neither Holland nor Kim teaches or suggests "a grid of conducting wires formed over and in electrical contact with the bias layer and configured to define an array of pixels corresponding to the array of doped gate regions" and "wherein the grid of conducting wires is configured to be electrically coupled to a voltage source and to distribute a bias voltage on the bias layer so as to bias the substrate with respect to the doped gate regions," as recited in claim 1.

The office action alleges that Kim teaches such a grid of conducting wires. However, OSM_2, referred to by the office action, is not a grid of conducting wires. Instead, Kim teaches "a plurality of first metals OSM_1 are formed over regions excluding the photo diodes and transfer gate electrodes PG_1 to PG_4 for shielding lights, and second metals OSM_2 connect between transfer gates having the same clock signals applied thereto of the transfer gates PG_1 to PG_4 formed repeatedly. Herein, the second metals OSM_2 are formed over each of the VCCD regions between the first metals OSM_1, with which layout the first, and the second metals OSM_1 and OSM_2 can shield lights incident to parts except the photo diode regions." (See column 5, lines 3-

14 of Kim). As shown in Figure 6, OSM_2 are a series of vertical lines that each connect to different transfer gates (through vias 7 of Figure 6; note the changing pattern of vias for each different OSM_2), but do not connect to each other electrically.

Therefore, Kim cannot be said to teach or suggest "a grid of conducting wires...wherein the grid of conducting wires is configured to be electrically coupled to a voltage source and to distribute a bias voltage on the bias layer so as to bias the substrate with respect to the doped gate regions." A series of vertical lines that do not connect to each other electrically, as taught in Kim, is not a grid of conducting wires and would not distribute a bias voltage on a bias layer, as the grid of conducting wires of claim 1 does.

Furthermore, even if Kim were to teach a grid of conducting wires, there is no motivation to provide such a grid in the CCD of Holland. The office action failed to present a prima facie case of obviousness by neglecting to provide a motivation to combine the references, stating only that "Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the charge coupled device of Holland by incorporating conducting wires to form electrical connections to the electrodes as taught by Kim." (See page 5 of the office action).

Applicants find no suggestion in either reference to provide such a grid. In Kim, Applicants find no discussion whatsoever of providing a bias voltage to a bias layer of a radiation detection device.

The only motivation to provide a detection device including a grid of conducting wires as provided in claim 1 comes from applicant's specification. The grid of claim 1 provides a number of benefits not found in Holland or Kim. The grid distributes the bias potential uniformly over the bias layer, while also serving to define pixels for the photodiode array. Additionally, the grid reduces the noise and improves immunity to external interferences. (See page 7, bottom paragraph, through page 8, top paragraph of the specification).

Since neither Kim nor Holland teaches a grid of conducting wires as recited in claim 1, and since the only motivation to provide such a grid comes from Applicant's specification, claim 1 is not obvious in view of the references. Therefore, for at least these reasons, claim 1 is patentable over Holland and Kim, alone or in combination.

Claims 2-17

Claims 2-17 depend from claim 1, and are therefore patentable for at least the same reasons stated above with respect to claim 1.

Claim 7

Claim 7 stands rejected as allegedly being unpatentable over Holland and Kim, and further in view of Cox. Applicants disagree.

Claim 7 is patentable for at least the additional reason that none of the references teach or suggest "a scintillation array comprising scintillation elements ... wherein the scintillation array includes optically reflective surfaces disposed between the scintillation elements to optically isolate one scintillation element from another," as recited in claim 7.

Instead, Cox teaches that "In accordance with other aspects of the invention, the scintillator comprises a glass plate doped with a phosphor. Alternately, the scintillator may be in the form of a fiber optic fiber, the core of which is doped with a phosphor. Another possibility is that the scintillator is in the form of a crystal phosphor deposited on the sensor array." (See column 1, line 64 to column 2, line 2).

Figure 7, cited in the office action, does not show such a scintillator array. Instead, element 402 appears to be a single scintillator, which may be one of the above types of scintillator (a glass plate doped with a phosphor, a fiber optic fiber with a phosphor doped core, or a crystal phosphor deposited on the sensor array).

Therefore, Cox does not teach a scintillator array as recited in claim 7. Neither Holland nor Kim remedy the deficiencies of Cox. Therefore, claim 7 is patentable for the additional reason that none of the references teach or suggest a scintillator array comprising scintillation elements.

Claim 19

Claim 19 stands rejected as being unpatentable over Holland in view of Kim. Applicants disagree.

Neither Holland nor Kim teaches or suggests "a grid of conducting wires proximate to and in electrical contact with the bias layer and configured to define an array of pixels corresponding to the array of photodiodes, wherein the grid of conducting wires is further configured to distribute a common potential to the photodiodes," as recited in claim 19.

At least because neither Holland nor Kim teaches or suggests such a grid of conducting wires, claim 19 is patentable over Holland and Kim alone or in combination. Further, for the same reasons as stated above with respect to claim 1, there is no motivation to combine Holland and Kim.

Claims 20-28

Claims 20-28 depend from claim 19, and are therefore patentable for at least the same reasons as stated above with respect to claim 19.

Claim 20

Claim 20 stands rejected as allegedly being unpatentable over Holland and Kim, and further in view of Cox. Applicants disagree.

Claim 20 is patentable for at least the additional reason that none of the references teach or suggest "a scintillation array of scintillation elements...wherein the scintillation array includes optically reflective surfaces disposed between the scintillation elements to optically isolate one scintillation element from another," as recited in claim 20. As stated above with respect to claim 7, neither Holland nor Kim remedy this deficiency. Therefore, claim 20 is patentable for this additional reason.

New claims 29 and 30

Applicants have added claims 29 and 30. No new matter is added. Support for these new claims can be found in originally filed claim 1, which is broadened in the current amendment.

Attached is a marked-up version of the changes being made by the current amendment.

CONCLUSION

For at least the above reasons, claims 1-30 are in condition for allowance. The foregoing comments with respect to positions taken by the Examiner cannot be construed as acquiescence by applicants with other positions of the Examiner that have not been explicitly contested. Similarly, the foregoing arguments for patentability of a claim cannot be construed as implying that there are not other good reasons for patentability of that claim or other claims. Should the Examiner have any questions concerning this response, the Examiner is invited to call the undersigned at (858) 678-5070.

Enclosed is a $146 check for excess claim fees and a 1 month the Petition for Extension of Time fee. Please apply any other charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: 8/8/02

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Version with markings to show changes made

In the claims:

Claims 1-8, 10, 11, 13, 15, 16, 18-21, and 24-28 have been amended as follows:

1. (Amended) A semiconductor position-sensitive radiation detection device, comprising:

a substrate formed of a semiconductor material doped to exhibit a first conductivity type and configured to have first and second surfaces opposing each other, the substrate having [(1) a transparent conducting bias electrode] a bias layer [formed over] proximate to the first surface and electrically coupled to the substrate,[and in electrical contact thereto] and [(2)] an array of doped gate regions of a second conductivity type [on] proximate to the second surface; and

a grid of conducting wires [formed over] proximate to and in electrical contact with the [conducting] bias [electrode] layer [or back contact layer on the first surface] and configured to define an array of pixels corresponding to the array of doped gate regions;

wherein the grid of conducting wires is [connected] configured to be electrically coupled to a voltage source and to distribute a [common potential] bias voltage on the [transparent conducting] bias [electrode] layer so as to bias the substrate with respect to the doped gate regions [to effect a photodiode array that receives radiation from the first surface].

2. (Amended) The device as in claim 1, wherein the [transparent conducting] bias [electrode] layer [is internal to the substrate and is formed by doping a layer of the substrate near] comprises a region of the substrate proximate to the first surface[to exhibit] that is more heavily doped with material of the first conductivity type than other regions of the substrate.

3. (Amended) The device as in claim 1, wherein the [transparent conducting] bias [electrode] layer [is external to the substrate and is formed from] comprises a transparent,

conductive [conductor] layer [externally attached to] formed proximate to the first surface.

4. (Amended) The device as in claim 3, wherein the [transparent back contact] bias layer includes a heavily-doped polycrystalline layer of [a] the semiconductor material [that forms the substrate].

5. (Amended) The device as in claim 1, wherein the [transparent conducting] bias [electrode] layer includes a first transparent, conductive layer [external to the substrate and formed from a transparent conductor layer externally attached to] formed on the first surface and a second layer comprising a region of the substrate proximate to the first surface that is more heavily doped with material of [internal to the substrate and formed by doping a layer of the substrate near the first surface to exhibit] the first conductivity type than other regions of the substrate.

6. (Amended) The device as in claim 1, further comprising a circuit layer [formed over] proximate to the second surface and configured to provide a gate contact to and a readout circuit for each doped gate region[,].

7. (Amended) The device as in claim 1, further comprising a scintillation array [of] comprising scintillation elements[formed in a scintillator crystal], said scintillation elements operable to convert incident radiation of a first wavelength [at a spectral range] outside [the] a characteristic spectral response range of the substrate into secondary photons [at] of a second wavelength within the characteristic spectral response range of the substrate, each of said scintillation elements aligned with and optically coupled to a corresponding one of the array of pixels, and [said scintillation array being coupled to the grid of conducting wires on the first surface of the substrate, wherein the scintillation elements match the size of and are aligned with the photodiodes of the photodiode array defined by the grid of conducting wires and] wherein the scintillation array includes

optically reflective surfaces disposed between the scintillation elements to optically isolate one scintillation element from another.

8. (Amended) The device as in claim 7, wherein one of the first and second conductivity types is [caused by] n-type [dopants] and the other is [caused by] p-type [dopants].

10. (Amended) The device as in claim 7, wherein the [transparent conducting] bias [electrode] layer [is internal to the substrate and includes] comprises a heavily-doped crystalline [layer] region of the substrate proximate to the first surface.

11. (Amended) The device as in claim 7, wherein the grid of conducting wires [is formed of] comprises a metallic material.

13. (Amended) The device as in claim 7, further comprising an anti-reflection layer [formed over the transparent conducting] proximate to the bias layer within each pixel and configured to reduce reflection of photons incident on the first surface.

15. (Amended) The device as in claim 13, wherein the anti-reflection layer includes a dielectric layer having a refractive index that has a relation with a refractive index of the [transparent conducting] bias layer.

16. (Amended) The device as in claim 1, wherein one of the first and second conductivity types is [caused by] n-type [dopants] and the other is [caused by] p-type [dopants].

18. (Amended) The device as in claim 7, further comprising an anti-reflection layer [formed over the transparent conducting] proximate to the bias layer within each pixel and configured to reduce reflection of photons incident on the first surface.

19. (Amended) A semiconductor position-sensitive radiation detection device, comprising:

an array of photodiodes formed in a substrate having a first surface and a second surface opposing the first surface, wherein a bias layer proximate to the first surface is electrically conducting to provide a common bias potential to the photodiodes and is optically transparent to receive input photons to be detected; and

a grid of conducting wires [formed over] proximate to and in electrical contact with the [first surface] bias layer and configured to define an array of pixels corresponding to the array of photodiodes, wherein the grid of conducting wires is [connected] further configured to distribute a common potential to the photodiodes.

20. (Amended) The device as in claim 19, further comprising a scintillation array of scintillation elements [formed in a scintillator crystal] operable to convert incident radiation at a first wavelength outside [the] a characteristic spectral response range of the photodiodes into secondary photons at a second wavelength within the characteristic spectral response range of the substrate and coupled to the grid of conducting wires [on the first surface of the substrate]proximate to the bias layer, each of said scintillation elements aligned with and optically coupled to a corresponding one of the array of pixels, and wherein [the scintillation elements match, and are aligned with, the pixels defined by the grid of conducting wires and] the scintillation array includes optically reflective surfaces disposed between the scintillation elements to optically isolate one scintillation element from another.

21. (Amended) The device as in claim 20, further incorporating an anti-reflection layer [formed over] proximate to the [first surface] bias layer within each pixel and configured to reduce reflection of photons incident to the first surface.

24. (Amended) The device as in claim 19, further incorporating an anti-reflection layer [formed over] proximate to the [first surface] bias layer within each pixel and configured to reduce reflection of photons incident to the first surface.

25. (Amended) The device as in claim 19, further comprising a circuit layer [formed over] proximate to the second surface and configured to provide [a gate contact to and, if provided, a readout circuit for each photodiode,] electrical contact with said array of photodiodes.

26. (Amended) The device as in claim 19, wherein the substrate is doped to exhibit a first conductivity type, and wherein the bias layer comprises a region of the substrate proximate to the first surface, where the region is heavily doped with a material of the first conductivity type. [the conductivity of the first surface is formed by doping a layer of the substrate near the first surface to exhibit the same conductivity as the substrate.]

27. (Amended) The device as in claim 19, wherein the [conductivity of the first surface the transparent is formed from] bias layer comprises a transparent conductor layer [externally attached to] formed proximate to the first surface.

28. (Amended) The device as in claim 27, wherein the substrate comprises a semiconductor material, and wherein the transparent conductor layer includes a heavily-doped polycrystalline layer of [a] the semiconductor material [that forms the substrate].